**Testing:**

**Analog**

1. **Simplified Circuit**
2. **Final Circuit**

**Digital**

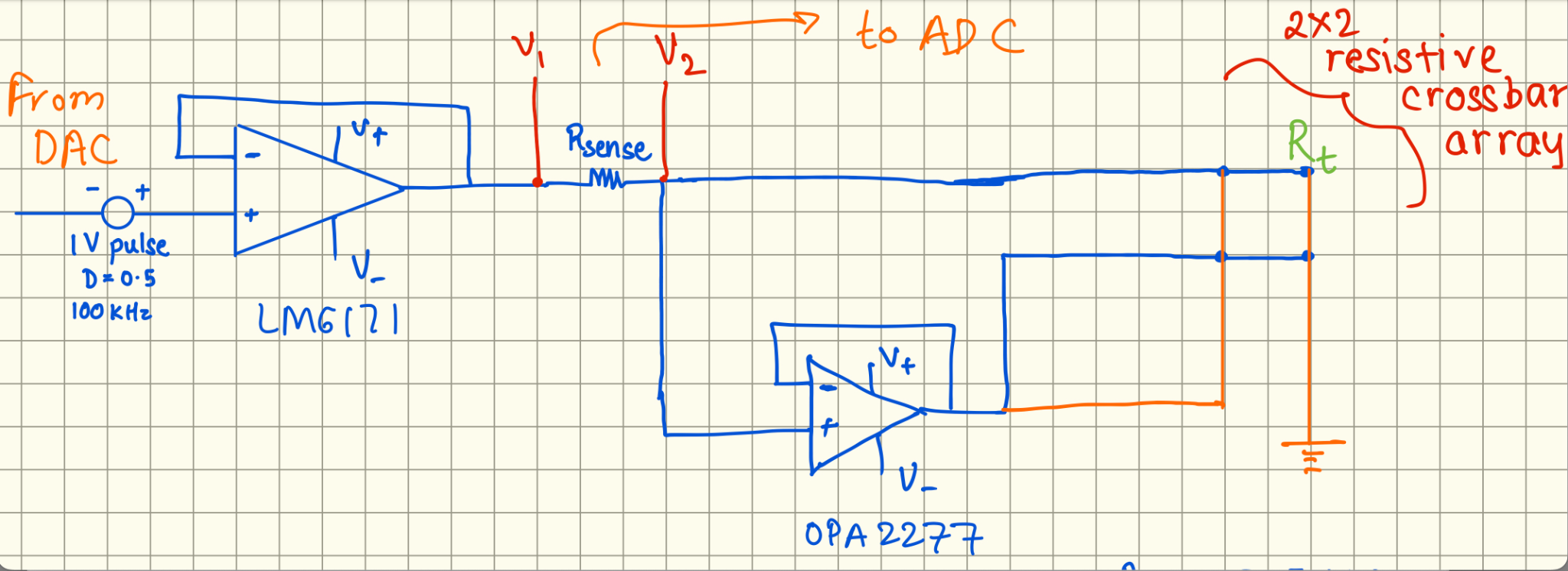
1. **Elementary and advanced ADC, DAC**
2. **FPGA and laptop communication**

**PCB**

1. **Simplified Circuit: in process of soldering and testing**
2. **Final Circuit: sent for fab**

**A. Simplified Circuit**:

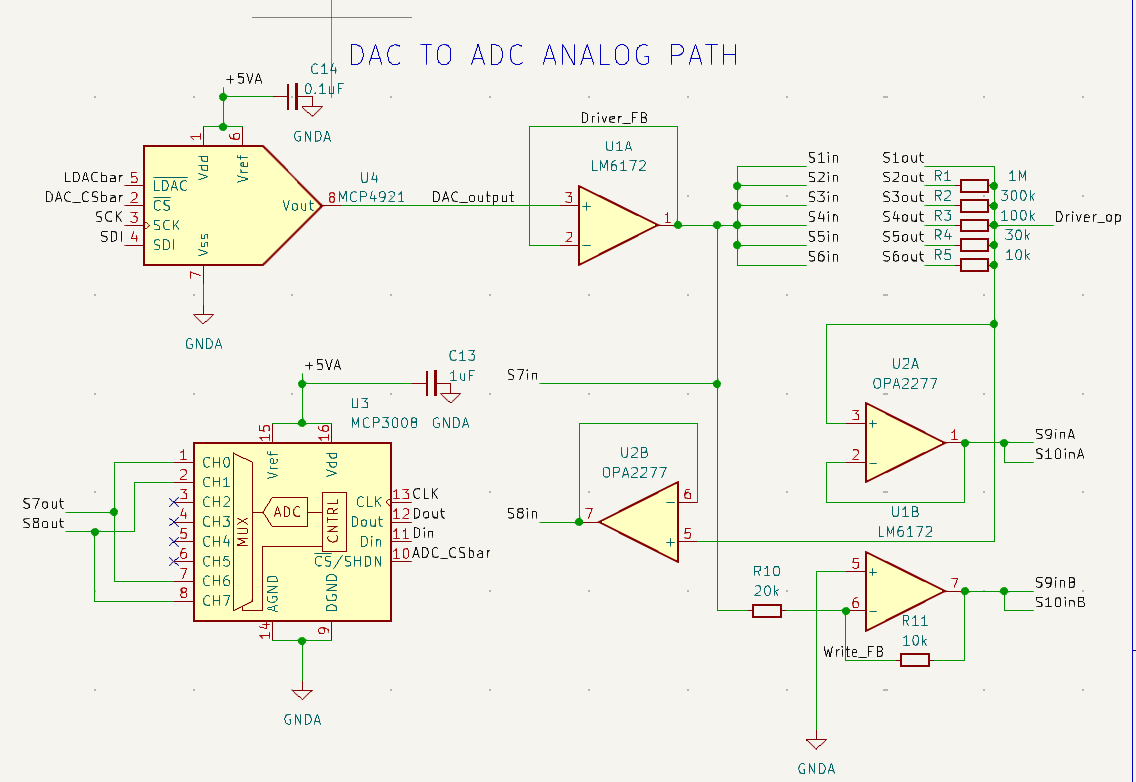
We designed a simplified circuit along with *elementary DAC and ADC* on 2 x 2 resistive crossbar array for the proof of concept of the flow and tested it .  
The testing was complete with sending a pulse of 100us from DAC and sampling the value at the correct instance of the pulse, measured by the ADC and displayed on the onboard LEDs of FPGA board.



This is the basic setup of the circuit that we tested for various frequencies and got correct resistance measurements with no sneak currents observed.

We got very good results for a square pulse of width 100 us.

We added a buffer amplifier before ADC in the PCB schematic for this simplified circuit along with all the switching circuitry and another amplifier for write operation.



We received this PCB on Monday at the end of the lab session.

**Ideal circuit flow**:

Schematic by hand: [Schematic\_hand.pdf](https://drive.google.com/file/d/19IjKuICe31It-q4dtc5-FK4axgM6YBKp/view?usp=share_link)

**Ideal op amps**:

We completed the entire schematic by hand for the ideal circuit that we wanted to get working.

We **tested each amplifier** of the **ideal** circuit individually at different frequencies and gains. We got the **current feedback amplifiers working**, however, we had to cancel this plan almost entirely due to an issue in DAC we observed while testing.

**Advanced DAC**

**Issue in DAC**: We got the DAC soldered, and while testing it, we observed that two pins were shorted. We desoldered it, but realized that the two pins were shorted internally. We **tried writing VHDL drivers and connecting current feedback amps** but it was not responding. Maheshwar sir said that one possible issue could be that the DAC got **damaged while soldering** because it was **ESD** sensitive.

**Advanced ADC**

We were able to get the **VHDL drivers for ADC working**, even though we had very less time left for final PCB submission by then. The differential **ADC responded initially**, however, the ADC got damaged during testing for a reason we could not pin point.

We had a spare ADC and could have tried on it again along with amplifiers, however, we had very less time remaining until the final PCB deadline and needed to finalize the design. Hence, we decided to stick with the simplified design version along with a few additional capabilities for our final design.

**FPGA and Laptop communication:**

We are **successfully able to send data from fpga to laptop and also send from laptop to fpga**. This has been demonstrated in the videos of Milestone 3.

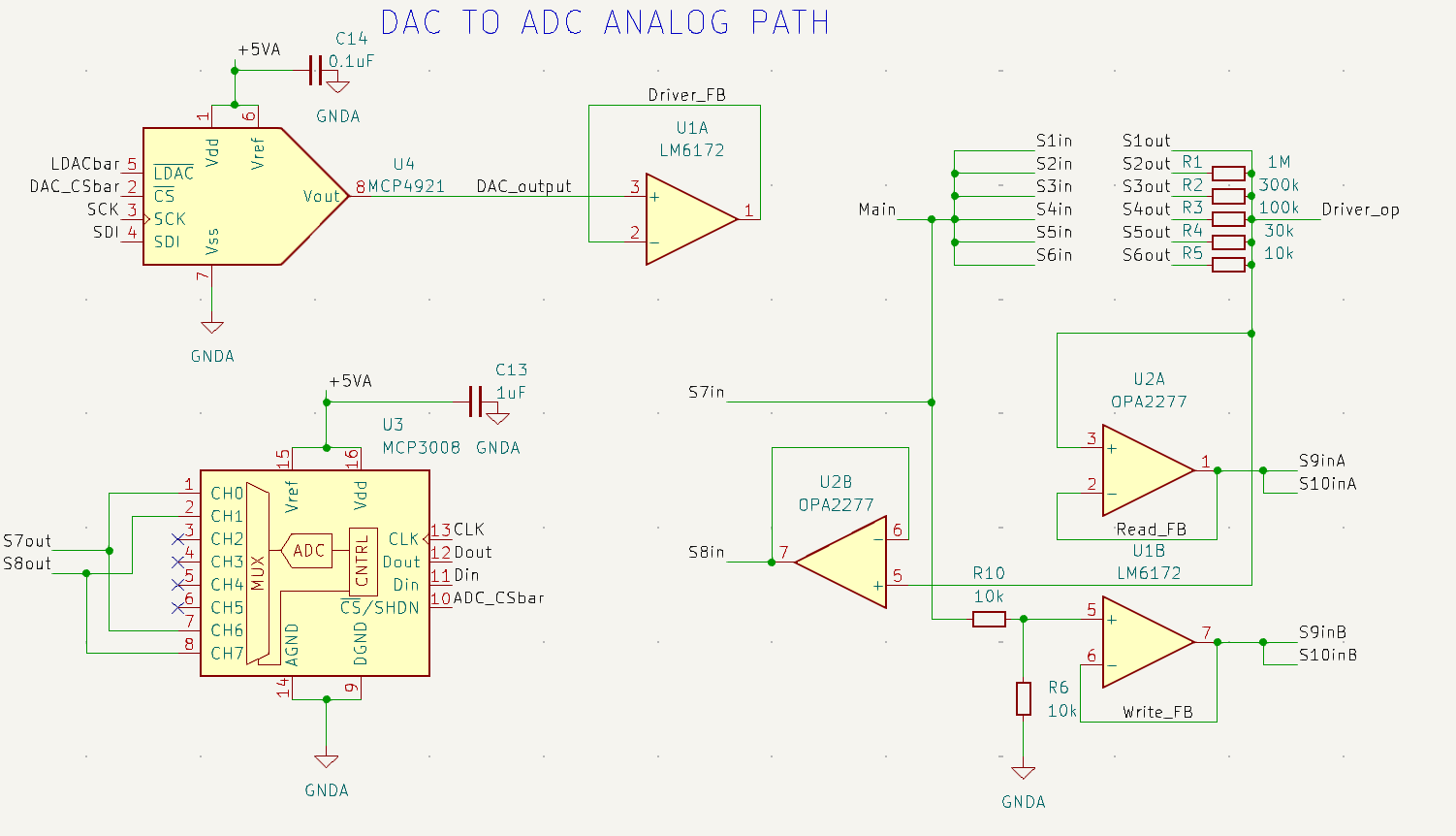
On the laptop, a simple python program that uses a library(needs quartus installed on the device) handles the communication, this is being integrated with a GUI.

Another challenge faced in programming was:

The jtag UART client on the FPGA which communicates with the Intel Avalon interface was written in verilog and drivers for ADC DAC in VHDL. A testing code was generated to perform **mixed synthesis of verilog and vhdl** files, and dumped onto the De0 Nano board, which worked **successfully**.

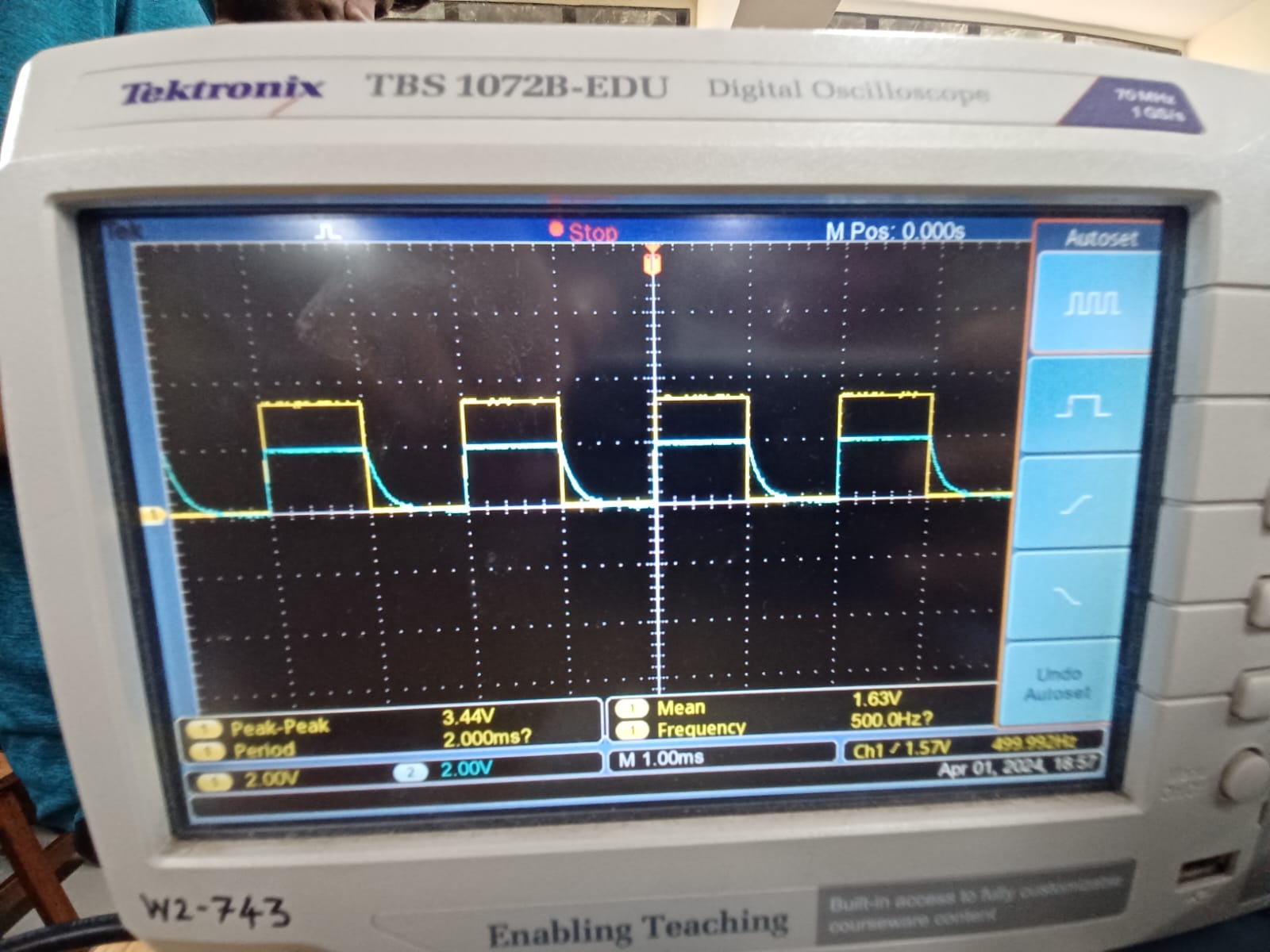
**B. Final circuit flow:**  
We added support for a -5V pulse to be sent. Moreover, we increased the size of the crossbar array to 3 x 3.

In the PCB, we rectified a mistake in the “write” buffer amplifier setup.



**Testing of switches:**

We want the switches to allow voltages from -5V to +5V. We didn’t have dual supply switches, but we managed to find CD4066 which takes positive supply of upto 20V with respect Vss(negative supply voltage). When working in 10V mode(that is desired since we need to run from -5V to +5V), the voltage at the control line needs to be less than +2V with respect to Vss for the switch to be open, that is, -3V with respect to circuit ground. But FPGA cannot provide -3V, hence, we tested the switch in 14V mode. Here, the switch is open at 0V and closed at 3.3V, as desired. We also tested its voltage rise time when the switch closes and it is of the order of nanoseconds, so that is not an issue. Hence, we will be supplying -5V and +9V to the switch.



**Power Supply**:

We have completed the schematic, **testing** and PCB design of the power circuit. All the components and the design works fine.